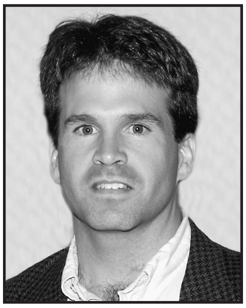
Session 19 Overview

Cellular and Multi-Mode Transceivers



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Associate Chair: Aarno Pärssinen, *Nokia, Helsinki, Finland*

After a slow ramp up, 3G cellular networks are beginning to be deployed in earnest. With data rates high enough to support painless mobile internet access, video phones, and other high-speed-data-enabled applications, the user experience is on the verge of a dramatic change. The increasing demand for wireless data places an unprecedented premium on spectral efficiency so that 3G standards include very stringent spectral emissions requirements. Further, as with any consumer application, low cost is essential. Meanwhile, 2G and 2.5G handsets sales continue to be robust with sales approaching 1 billion units per year and with growing markets in the third world cost pressures are unceasing. Still further, consumers demand continuous connectivity though sometimes incompatible networks, so the demand for multi-mode transceivers is growing. These challenges, and more, are addressed by the papers in this session.

Our first two papers address the problem of achieving high spectral purity *and* low cost. Since WCDMA phones need to simultaneously transmit high power signals and receive very low-power signals, it is necessary to suppress the transmitter's noise such that it is well below the receiver's noise in order to prevent desensitizing the receiver. To date, a typical WCDMA transmitter's SNR is between 145 and 150dBc/Hz in the receive channel at 190MHz offset. This level of noise dictates the inclusion of a SAW filter in the transmit path. Papers 19.1 by Analog Devices and 19.2 by ACP Zurich and ETHZ use completely different techniques to produce unprecedented spectral purity with SNRs of 163dBc/Hz in the case of Paper 19.1 and 156cdB/Hz in the case of 19.2. These transmitters enable the elimination of the TX SAW filters for further cost reduction and miniaturization.

Paper 19.3 from Nokia addresses the challenge of cost reduction by employing an architecture that is amenable to integration in digital CMOS. A direct-digital RF modulator is particularly challenging for WCDMA applications because of the very large power control range requirement.

Coexistence with 1st-generation analog cellular systems in the US makes CDMA2000 a particularly difficult 3G standard – especially with respect to receiver linearity and local oscillator phase noise. Paper 19.4 from Danube IC Engineering and Infineon is the first published highly integrated transceiver for this standard.

Paper 19.5 from Comlent, Orange Coast Semiconductor, and U Florida is the first paper describing a transceiver for TD-SCDMA – a Chinese cellular standard that is a TDD version of WCDMA.

The extremely difficult challenge of software-defined radio is addressed in Paper 19.6 by IMEC, Samsung, and U Lecce. The authors use external MEMS switches to enable band-select filters thus reducing the linearity and power dissipation requirements in the transceiver.

Cost reduction for GSM/EDGE handsets is a never-ending goal. Paper 19.7 from Hitachi and Renesas describes a polar-loop transmitter for EDGE with the power amplifier controller integrated. The transceiver includes integrated ADCs and DACs enabling a completely digital baseband processor IC.

The linearity required of a WCDMA transmitter results in relatively low power amplifier efficiency. Paper 19.8 from Sony describes an analog-domain pre-distortion technique that enables lower power amplifier backoff and thus better efficiency.

Our final paper, Paper 19.9 by U Michigan, describes a PLL-based modulator with a novel digital phase detector without the inverter-delay resolution limit of previously published efforts. This wideband modulator is well suited to multi-mode and low-power transmitters.

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19.1 Direct-Conversion WCDMA Transmitter with -163dBc/Hz Noise at 190MHz Offset **1:30 PM**

B. Tenbroek, Analog Devices, West Malling, United Kingdom

A direct-conversion multi-band TX for 1710 to 2025MHz is implemented in a 0.18µm CMOS process with post-passivation inductors. An on-chip balun and noise of -163dBc/Hz at 190MHz offset enable the PA to be driven directly with no SAW filter. A tapped attenuator provides >60dB gain control at RF.

19.2 A Linear Uplink WCDMA Modulator with -156dBc/Hz Downlink SNR **2:00 PM**

D. Papadopoulos, ACP, Zurich, Switzerland

A linearity-boosting technique for upconversion mixers enables a 0.13µm CMOS WCDMA modulator to achieve -49dBc ACLR and -156dBc/Hz SNR. The chip consumes 113mW from a 1.2V supply. It is suitable for SAW-filter-free TX implementations. Results show that this technique improves the mixer IIP3 by 6dB.

19.3 A WCDMA Transmitter in 0.13µm CMOS Using Direct-Digital RF Modulator **2:15 PM**

P. Seppinen, Nokia, Helsinki, Finland

A WCDMA transmitter based on direct-digital RF modulator has a power control range of >90dB and achieves an ACPR of -58dBc with a channel power of -2dBm. Using an external PA with a power gain of 27dB, the measured EVM is <2% with signal levels from -35 to +25dBm. The chip is fabricated in a 0.13µm 1.2V CMOS process and occupies 4mm^2.

19.4 A Single-Chip Dual-Band CDMA2000 Transceiver in 0.13µm CMOS **2:30 PM**

J. Zipper, Danube Integrated Circuit Engineering, Linz, Austria

A single-chip dual-band transceiver for CDMA2000 is presented. For PCS, the zero-IF receiver achieves an NF of 9dB and an IIP3 of 0.5dBm at 32dB gain resulting in a maximal output SNR of 23dB. The key figures of merit for the transmitter are +13.5dBm maximum output power, ACPR1=-57dBc and ACPR2=-69dBc while drawing 34mA average current in typical environment.

19.5 A Dual-Band CMOS Transceiver for 3G TD-SCDMA **3:15 PM**

Z. Li, Comlent Communications, Shanghai, China

A TD-SCDMA transceiver is integrated in a 0.18µm CMOS process. The RX achieves 62dB voltage gain, 3.2dB NF, and -14.5dBm IIP3. The TX achieves 3.7% EVM with -46dBc ACLR at +4.4dBm maximum output power. On-chip fractional-N PLL has 0.85° jitter and spurs below 77dB. The RX and TX consume 95mW and 158mW, respectively.

19.6 A Fully Reconfigurable Software-Defined Radio Transceiver in 0.13µm CMOS **3:45 PM**

J. Craninckx, IMEC, Leuven, Belgium

A fully reconfigurable SDR contains an RX, a TX, and 2 synthesizers for true multi-standard operation. A MEMS-enabled dual-band LNA proves the feasibility of switched antenna filtering for interference robustness. The baseband section is programmable in noise level and in bandwidth from 350kHz to 23MHz. The receiver has 6dB NF, -9dBm IIP3, and up to 90dB gain. Implemented in a 0.13µm CMOS process, it draws 62mA to 120mA in RX mode and 56mA to 89mA in TX mode from a 1.2V supply.

19.7 A Polar Loop Transmitter with Digital Interface including a Loop-Bandwidth Calibration System **4:15 PM**

Y. Akamine, Hitachi, Tokyo, Japan

An RFIC with digital interface for GSM/EDGE is presented. The architecture is a polar loop transmitter and a direct conversion receiver. The transmitter draws 100mA in GSM and 130mA in EDGE modes. A loop-bandwidth calibration system that can keep the variation of the loop bandwidth to less than ±10% after a few microseconds calibration period is applied. The RFIC also contains a timing-control circuit to avoid having a zero PA output amplitude during the switching between GSM and EDGE.

19.8 A Polynomial-Predistortion Transmitter for WCDMA **4:45 PM**

N. Mizusawa, Sony, Tokyo, Japan

A 0.18µm SiGe BiCMOS WCDMA handset transmitter IC implements a 5th-order analog baseband complex-polynomial predistorter. The IC reduces the power consumption of the GaAs HBT PA for the 1.9GHz WCDMA handset by 18% and raises the maximum output power by 1.5dB. At 0dBm output power, the IC consumes 64mA and 57mA from a 2.4V supply with and without predistortion, respectively.

19.9 A 14mW Fractional-N PLL Modulator with Enhanced Digital Phase Detector and Frequency-Switching Scheme **5:00 PM**

M. Ferriss, University of Michigan, Ann Arbor, MI

A 2.2GHz fractional-N synthesizer with a digital phase detector and a dual switching scheme is presented. An additional feedback loop incorporating phase oversampling helps to achieve a measured noise performance of -133dBc (-106dBc) at a 10MHz (1MHz) offset. The MSK modulation rate is 927.5kb/s. The 0.7mm^2 prototype IC, implemented in a 0.13µm CMOS process, consumes 14mW from a 1.4V supply.